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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,910	07/18/2003	Nhon Quach	42390P8139C	2824

7590 01/24/2006

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EXAMINER	
MCCARTHY, CHRISTOPHER S	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,910	QUACH, NHON	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. Claims 1-5, 8 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6, 17 of U.S. Patent No. 6,625,749. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is well settled that the omission of an element and its function is an obvious expedient if elements perform the same function (In re Karlson, 136 USPQ 184 CCPA 1973).

Claim 1 omits the following element from patented claim 1: a main memory, wherein the recovery routine saves the uncorrupted processor state data to an uncacheable portion of the main memory system.

Clams 2-5 are disclosed in patented claims 2,3,5,6, respectively.

Claim 8 omits the following element from patented claim 17: wherein recovering the minimal set of processor state data comprises replacing corrupted processor state data from one of the execution cores with uncorrupted processor state data saved from the other of the execution cores.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Klecka et al. U.S. Patent 6,393,582.

As per claim 1, Klecka teaches a computer system comprising: a processor having first and second execution cores and a check unit (column 2, line 66 – column 3, line 3), the first and second execution cores to process instructions independently when the processor is in a split mode (column 6, lines 37-43) and to process identical instructions in lock step when the processor is in a redundant mode (column 4, lines 40-44), and the check unit to compare results from the first and second execution cores when the processor is in redundant mode (column 4, lines 50-65); and a non-volatile memory (column 3, lines 6-9; column 6, lines 28-36) in which is stored a recovery routine that switches the processor to split mode when the check unit detects an error (column 5, lines 15-25; column 6, lines 28-36), identifies uncorrupted processor state data from at least one of the execution cores (column 6, lines 37-61), and initializes the first and second execution cores with the identified processor state data (column 6, lines 37-61; column 5, lines 22-25).

As per claim 2, Klecka teaches the computer system of claim 1, wherein the error recovery routine returns the processor to the redundant mode (column 7, lines 37-44).

As per claim 3, Klecka teaches the computer system of claim 1, wherein the error recovery routine identifies uncorrupted processor state data in selected storage structures associated with each execution core (column 6, lines 22-35), copies the uncorrupted processor

state data to a specified memory location (column 7, lines 23-25), and reconciles the copied processor state data, when the processor enters split mode (column 7, lines 26-29).

As per claim 4, Klecka teaches a method for handling soft errors (column 3, lines 37-44) in a processor capable of operating first and second execution cores in redundant and split modes, the method comprising: detecting a soft error when the processor is operating in the redundant mode (column 3, lines 37-44); executing an error recovery routine on each execution core to save uncorrupted data from storage structures associated with the first and second execution cores, wherein the error recovery routine is stored in a non-volatile memory (column 6, lines 22-36); and recovering processor state data from the saved uncorrupted data (column 7, lines 22-29).

As per claim 5, Klecka teaches the method of claim 4, further comprising: reconciling the saved, uncorrupted data to recover the processor state data (column 7, lines 26-29); and initializing the first and second execution cores using the recovered processor state data (column 6, lines 37-61; column 5, lines 22-25).

As per claim 6, Klecka teaches a machine readable medium (column 3, lines 6-9) on which are stored instructions that are executable by a dual execution core processor to implement a method for recovering from soft errors (column 3, liens 37-44), the method comprising: switching the processor to operate the dual execution cores independently when a soft error is detected (column 6, lines 37-61; column 3, lines 37-44); executing an error recovery routine on each of the execution cores to recover a minimum set of processor state data from uncorrupted processor state data (column 6, lines 22-35), wherein the error recovery routine is stored in a

non-volatile memory (column 3, lines 6-9; column 6, lines 28-36); and initializing each of the dual execution cores, using the minimum set of processor state data (column 5, lines 22-25).

As per claim 7, Klecka teaches the machine readable medium of claim 6, wherein initializing each of the dual execution cores comprises: switching the processor to operate the dual execution cores in lock step; and copying the minimum set of processor state data to each of the dual execution cores (column 7, lines 37-44; column 5, lines 22-25).

As per claim 8, Klecka teaches a computer system comprising: a processor having first and second execution cores that operate in lock step when the processor is in a redundant execution mode (column 4, lines 40-45) and operate independently when the processor is in a split execution mode (column 6, lines 37-45); and a non-volatile memory in which are stored instructions that may be implemented by the processor to implement a method for recovering from soft errors when the processor is in redundant execution mode (column 3, lines 6-9; column 5, lines 15-25), the method comprising: switching the processor to split execution mode (column 6, liens 37-61); saving uncorrupted processor state data from each execution core to a designated memory location (column 6, lines 22-35); recovering a minimal set of processor state data from the saved, uncorrupted processor state data (column 7, lines 22-29); and initializing each execution core with the minimal set of processor state data (column 5, lines 22-25).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
January 13, 2006